



- ☐ Tentative Specification
- ☐ Preliminary Specification
- ☒ Approval Specification

MODEL NO.: V562D1
SUFFIX: L04

Customer:

APPROVED BY

SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver 2.0	Apr.25,'11	All	All	Approval Specification is first issued.
www.panelook.com				



1. GENERAL DESCRIPTION

1.1. OVERVIEW

V562D1-L04 is a 56" Thin-Film-Transistor Liquid-Crystal (TFT-LCD) module with one 32-CCFL backlight unit and 8ch-LVDS interface utilization. This module supports 3840 x 2160 Quad Full High Definition (QFHD) TV format and can display 1G colors (10-bit). The inverter module for backlight is also built-in.

1.2. FEATURES

Ultra Wide Viewing Angle (176(H)/ 176(V) for CR>30)
High Brightness (450 nits)
High Contrast Ratio (1200:1)
Ultra Fast Response Time (Gray to gray average 6.5 ms)
High Color Saturation (NTSC 100%)
Contrasty Image (Gamma 2.5)
QFHD (3840 x 2160 pixels) Resolution
8ch-LVDS (Low Voltage Differential Signaling) Interface
RoHS Compliance

1.3. APPLICATION

Luxurious Living Room TVs
Public Display
Home Theater
Satellite Communication
Medical Analyses/ Instruction
Security and Monitoring
Industrial Design
3D Display
Digital Museum
Multi-Media Display

1.4. GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1244.16 (H) x 699.84 (V) (56.2" diagonal)	mm	(2)
Bezel Opening Area	1252.1 (H) x 707.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840x R.G.B. x 2160	pixel	-
Pixel Pitch(Sub Pixel)	0.108 (H) x 0.324 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1G colors (10-bit)	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Hard & Glare coating,Hardness 3H	-	(1)

Note (1) The specifications of the surface treatment are temporarily for this phase. CMI reserves the rights to change this feature.

**1.5. MECHANICAL SPECIFICATIONS**

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	1309	1309.5	1310.2	mm	
	Vertical(V)	766.5	767	767.7	mm	
	Depth(D)	57.2	58.5	59.8	mm	To PCB cover
	Depth(D)	61.9	63.2	64.5	mm	To inverter cover
Weight		23000	23500	24000	g	

2. ABSOLUTE MAXIMUM RATINGS

2.1. ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+55	°C	(1)
Operating Ambient Temperature	T _{OP}	0	45	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	X, Y axis	30	G	(3), (5)
		Z axis	30	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40\text{ }^{\circ}\text{C}$).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ }^{\circ}\text{C}$).

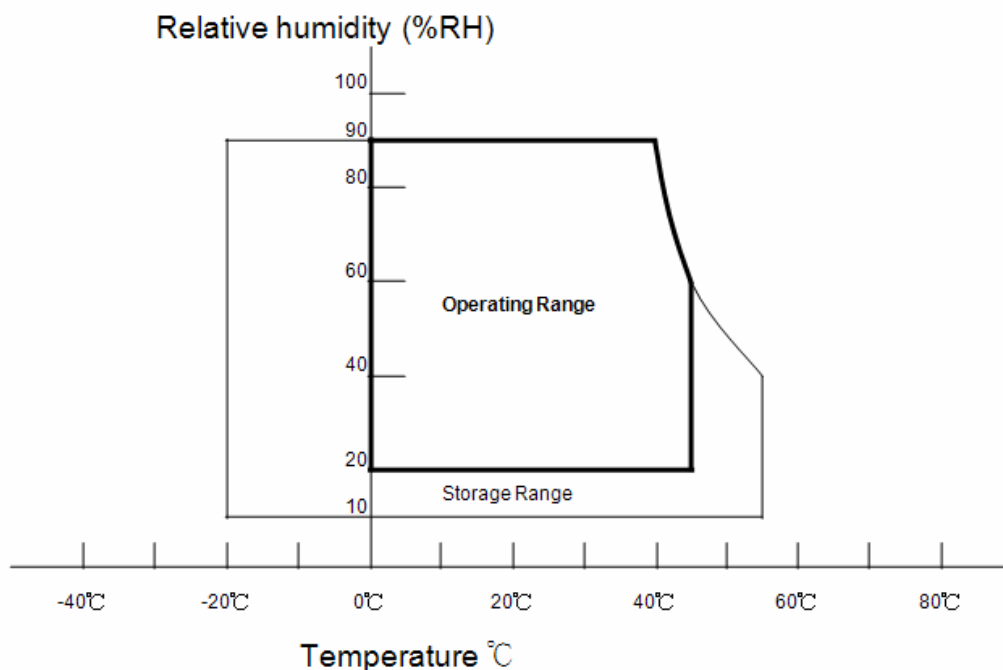
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, and $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture. The module would not be twisted or bent by the fixture.



**2.2. RATINGS OF IMAGE STICKING**

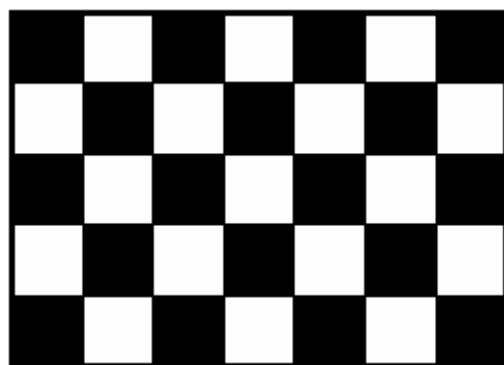
Item	Symbol	Value	Unit	Note
Room Temperature Image Sticking	RT IS	Invisibility	6% ND (%)	(1)(3)
High Temperature Image Sticking	HT IS	Invisibility	6% ND (%)	(2)(3)

Note (1) Room temperature image sticking test is at $25\pm3^{\circ}\text{C}$ environment and fix the pattern A (checker pattern) for 12 hours.

Note (2) High temperature image sticking test is at $50\pm3^{\circ}\text{C}$ environment and fix the pattern A for 12 hours.

Note (3) Inspection condition is at pattern B (512grade) after 5 mins from pattern A.

A. Pattern A (checker pattern)



B. Pattern B (512grade)

**2.3. PACKAGE STORAGE**

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

3. ELECTRICAL MAXIMUM RATINGS

3.1. TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC1}	-0.3	20	V	(1)
	V_{CC2}	-0.3	6	V	
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under normal operating conditions.

3.2. BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	5000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (2)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

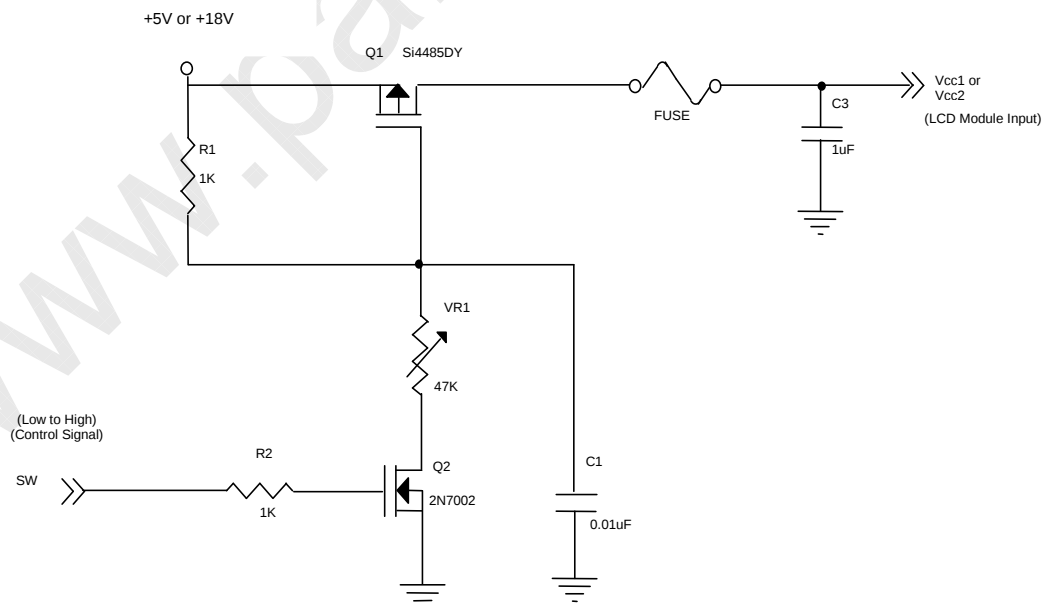
Note (2) The control signals include On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

4. ELECTRICAL CHARACTERISTICS**4.1. TFT LCD MODULE**

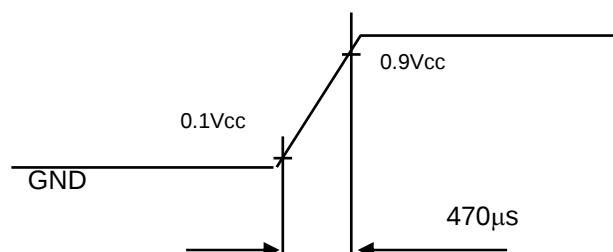
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC1}	17.1	18	18.9	V	(1)
		V _{CC2}	4.5	5	5.5	V	
Power Supply Ripple Voltage		V _{RP1}	-	-	400	mV	
		V _{RP2}	-	-	200	mV	
Rush Current		I _{RUSH1}	-	-	8	A	(2)
		I _{RUSH2}	-	-	7.5	A	
Power Supply Current	White	I _{CC1}	-	4.2	4.7	A	(3)
	Black		-	1.8	-	A	
	Vertical Stripe		-	3.5	-	A	
	White	I _{CC2}	-	5	-	A	
	Black		-	4.9	-	A	
	Vertical Stripe		-	5.4	5.9	A	
LVDS Interface	Differential Input High Threshold Voltage	V _{LVTH}	-	-	+100	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	-100	-	-	mV	
	Common Input Voltage	V _{CM}	1.125	1.25	1.375	V	
	Differential Input Voltage (single-end)	V _{ID}	200	-	600	mV	
	Terminating Resistor	R _T	-	100	-	ohm	
CMOS Interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement conditions:

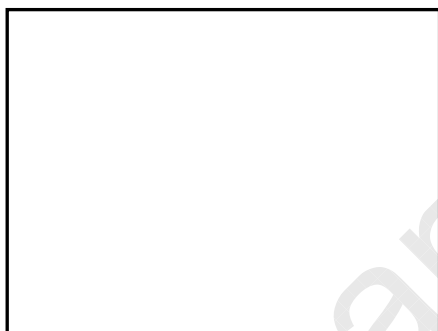


Vcc rising time is at least 470 μ s



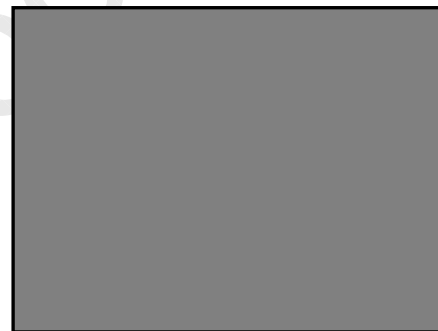
Note (3) The specified power supply current is under the conditions at Vcc1 = 18 V, Vcc2 = 5 V, Ta = 25 $\pm$ 2 $^{\circ}$ C, fv = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



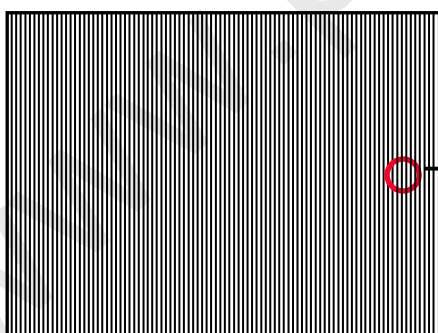
Active Area

b. Black Pattern

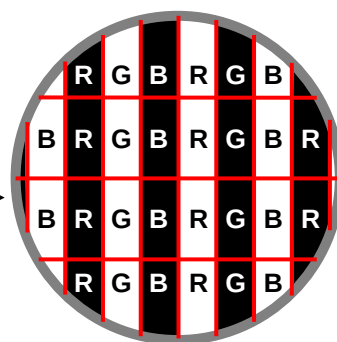


Active Area

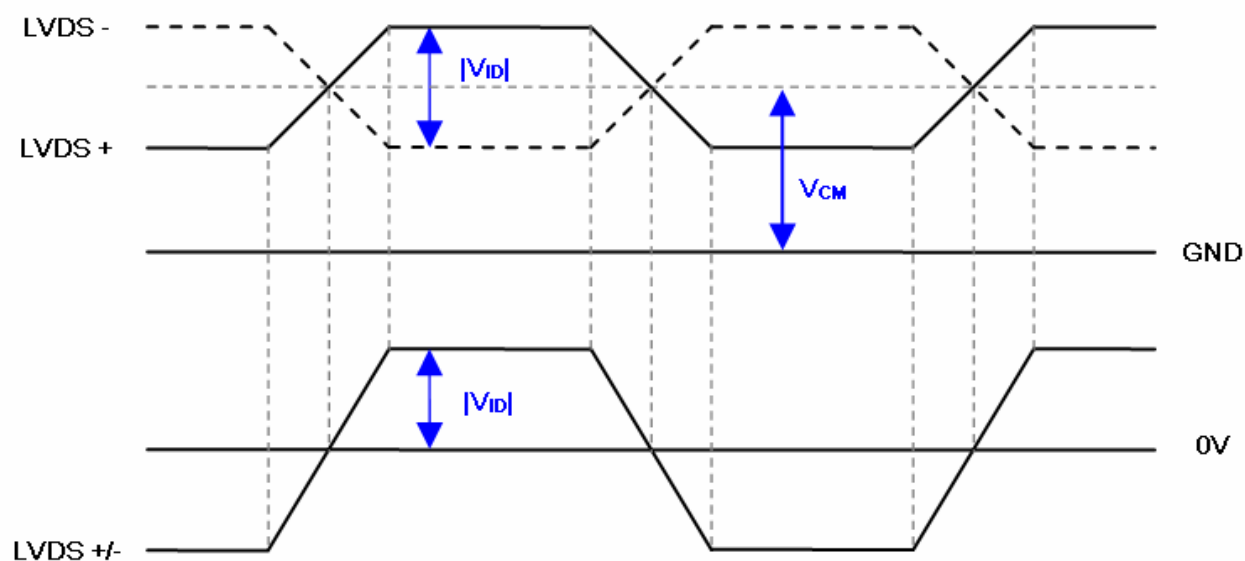
c. Vertical Stripe Pattern



Active Area



Note (4) LVDS input signal waveform



4.2. BACKLIGHT UNIT

4.2.1. CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS

(Ta=25±2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	VW	-	1728	-	VRMS	IL =6.0mA
Lamp Current	IL	5.5	6.0	6.5	mARMS	(1)
Lamp Starting Voltage	VS	-	-	2550	VRMS	(2), Ta = 0 °C
		-	-	2350	VRMS	(2), Ta = 25 °C
Operating Frequency	Fo	47	50	53	KHz	(3)
Lamp Life Time	LBL	-	50000	-	Hrs	(4)

4.2.2. INVERTER CHARACTERISTICS

(Ta=25±2 oC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	PBL	-	322	339	W	(5),(6) IL = 6.3 mA
Power Supply Voltage	VBL	22.8	24.0	25.2	VDC	
Power Supply Current	IBL	-	13.4	14.2	A	Non Dimming
Input Inrush current	-	-	-	19.7	A	(7)
Input Ripple Noise	-	-	-	912	mVP-P	VBL=22.8V
Oscillating Frequency	FW	47	50	53	KHz	(3)
Dimming Frequency	FB	150	160	170	Hz	
Minimum Duty Ratio	DMIN	-	20	-	%	

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board

Note (2) The lamp starting voltage VS should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

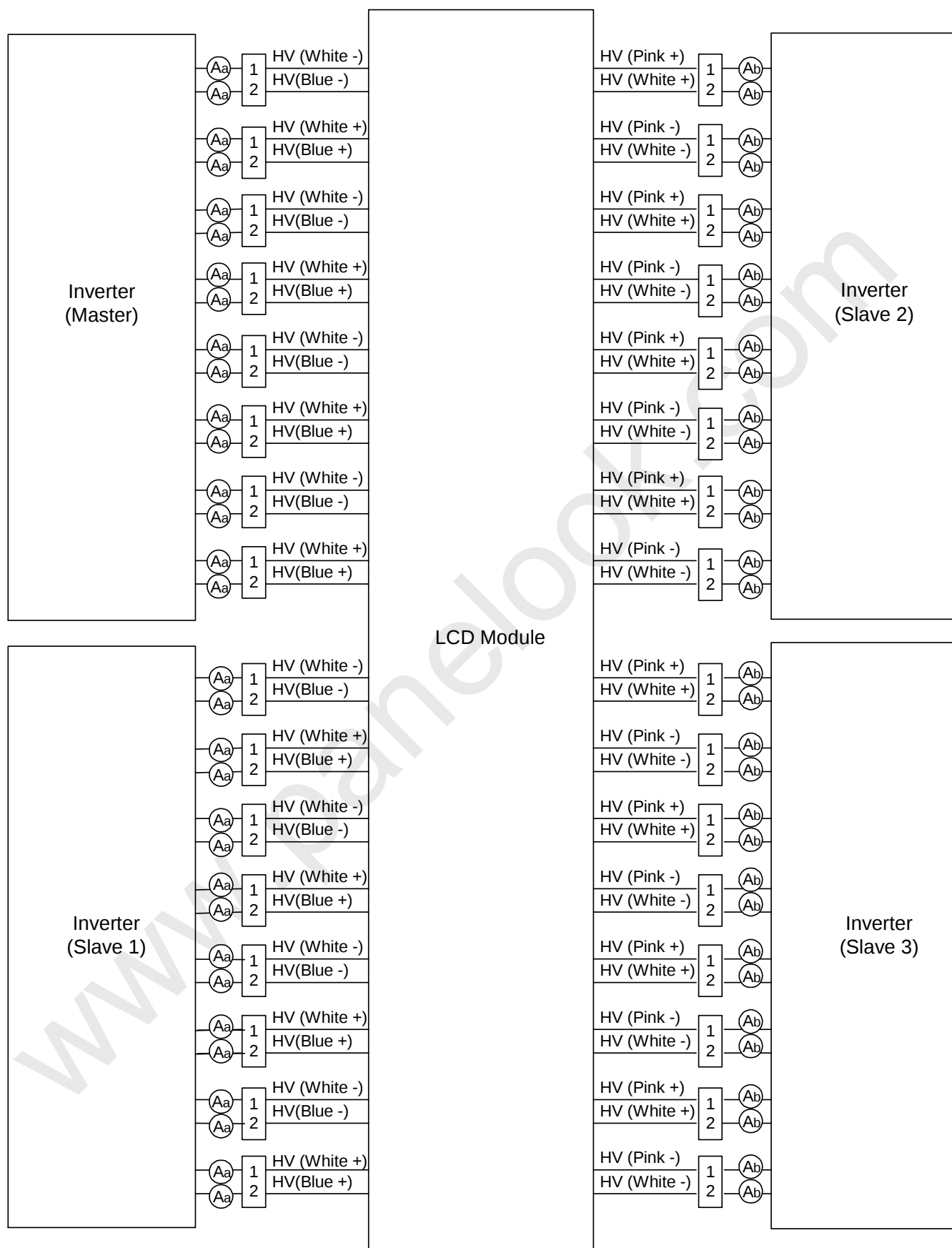
Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2 °C and IL = 5.5 ~ 6.5mA rms.

Note (5) The power supply capacity should be higher than the total inverter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 56" backlight unit under input voltage 24V, average lamp current 6.3 mA and lighting 30 minutes later.

Note (7) The duration of Input Inrush Current is about VBL Rising Time 30ms.



4.2.3. INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—	5.0	V	Ext. Dim. Control
	LO		—	0	—	0.8	V	Int. Dim. Control
Internal PWM Control Voltage	MAX	V_{IPWM}	$V_{SEL} = L$	2.85	3.0	3.15	V	Maximum duty ratio
	MIN			—	0	—	V	Minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	$V_{SEL} = H$	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty off
VBL Rising Time		$Tr1$	—	30	—	—	ms	10%-90% V_{BL}
VBL Falling Time		$Tf1$	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	M Ω	
PWM Delay Time		T_{PWM}	—	0	—	—	mS	
BLON Delay Time		T_{on}	—	300	—	—	ms	
		T_{on1}	—	300	—	—	ms	
BLON Off Time		T_{off}	—	300	—	—	ms	

Note (1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure.

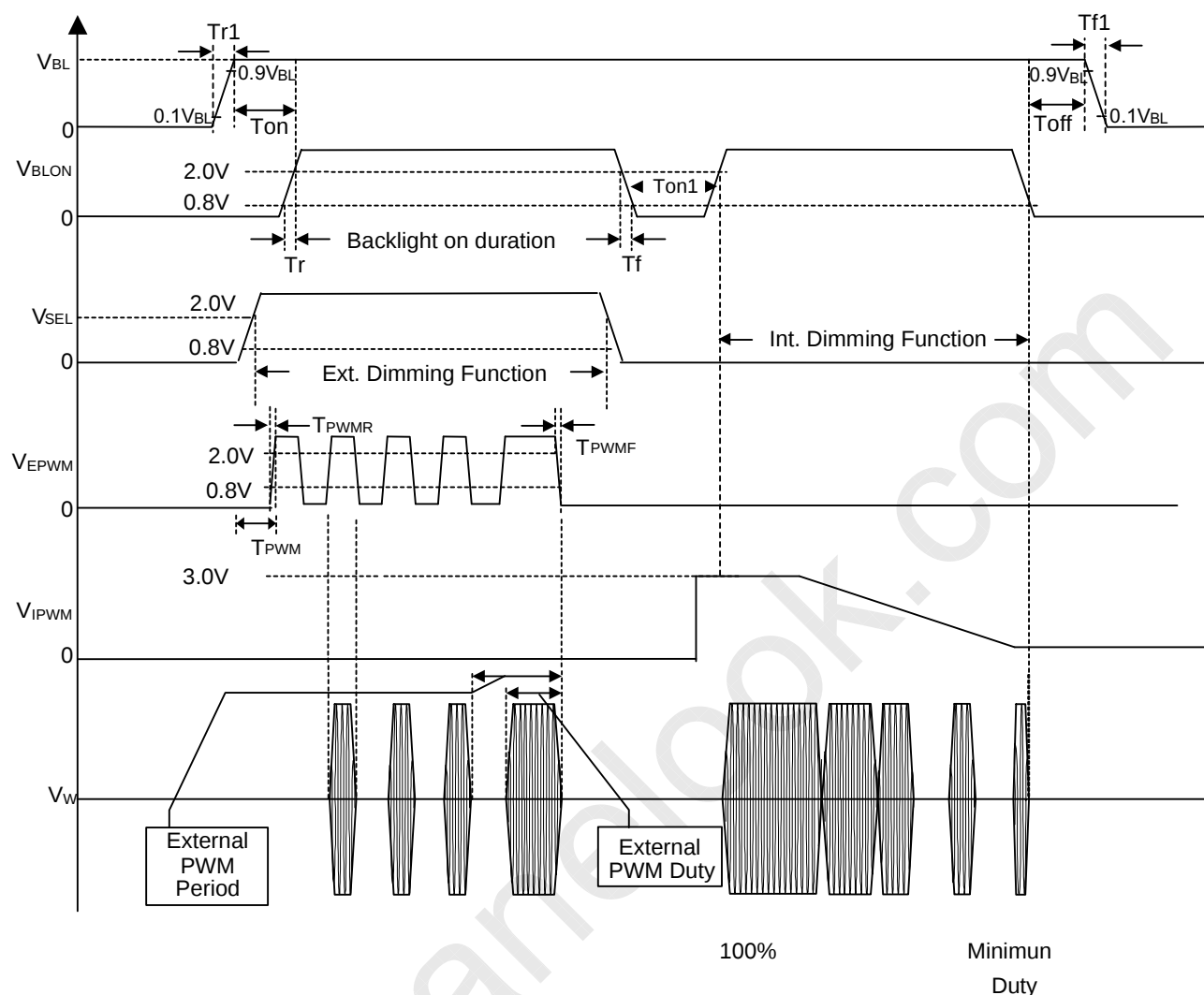
Note (3) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (4) Abnormal operation may occur if these maximum values of control signal are exceeded.

Note (5) While system is turned ON or OFF, the power sequences must follow as below descriptions:

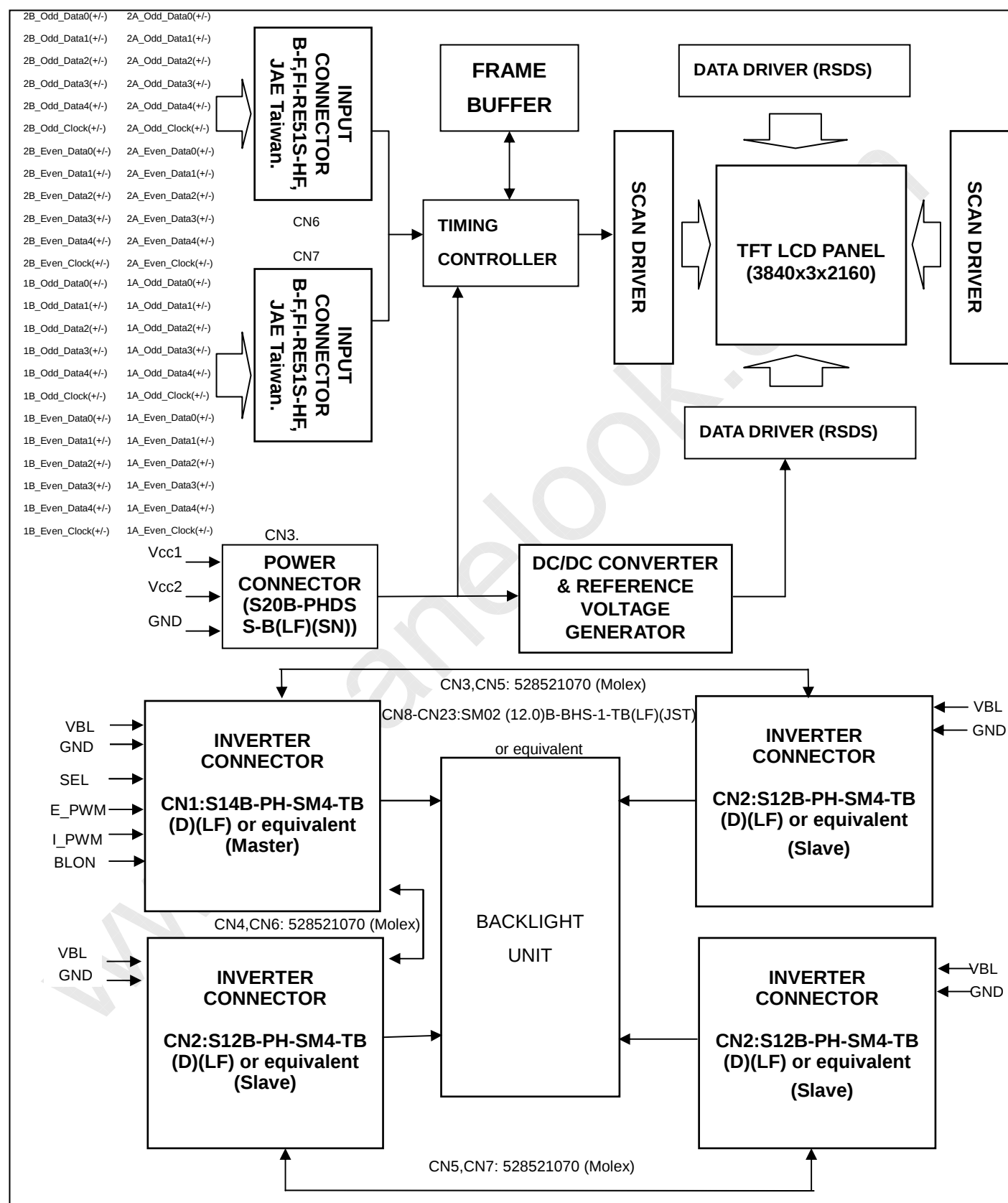
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



5. BLOCK DIAGRAM

5.1. TFT LCD MODULE



6. LCD INPUT TERMINAL PIN ASSIGNMENT

6.1. TFT LCD MODULE L.V.D.S. INPUT

CN6 Connector Pin Assignment

Pin No.	Name	Description	Note
1	GND	Ground.	
2	2B_SRX0-	Negative transmission data of Second pixel 0.	
3	2B_SRX0+	Positive transmission data of Second pixel 0.	
4	2B_SRX1-	Negative transmission data of Second pixel 1.	
5	2B_SRX1+	Positive transmission data of Second pixel 1.	
6	2B_SRX2-	Negative transmission data of Second pixel 2.	
7	2B_SRX2+	Positive transmission data of Second pixel 2.	
8	2B_SCLK-	Negative of Second clock.	
9	2B_SCLK+	Positive of Second clock.	
10	2B_SRX3-	Negative transmission data of Second pixel 3.	
11	2B_SRX3+	Positive transmission data of Second pixel 3.	
12	2B_SRX4-	Negative transmission data of Second pixel 4.	
13	2B_SRX4+	Positive transmission data of Second pixel 4.	
14	2B_FRX0-	Negative transmission data of First pixel 0.	
15	2B_FRX0+	Positive transmission data of First pixel 0.	
16	2B_FRX1-	Negative transmission data of First pixel 1.	
17	2B_FRX1+	Positive transmission data of First pixel 1.	
18	2B_FRX2-	Negative transmission data of First pixel 2.	
19	2B_FRX2+	Positive transmission data of First pixel 2.	
20	2B_FCLK-	Negative of First clock.	
21	2B_FCLK+	Positive of First clock.	
22	2B_FRX3-	Negative transmission data of First pixel 3.	
23	2B_FRX3+	Positive transmission data of First pixel 3.	
24	2B_FRX4-	Negative transmission data of First pixel 4.	
25	2B_FRX4+	Positive transmission data of First pixel 4.	
26	GND	Ground.	
27	2A_SRX0-	Negative transmission data of Second pixel 0.	
28	2A_SRX0+	Positive transmission data of Second pixel 0.	
29	2A_SRX1-	Negative transmission data of Second pixel 1.	
30	2A_SRX1+	Positive transmission data of Second pixel 1.	
31	2A_SRX2-	Negative transmission data of Second pixel 2.	
32	2A_SRX2+	Positive transmission data of Second pixel 2.	
33	2A_SCLK-	Negative of Second clock.	
34	2A_SCLK+	Positive of Second clock.	
35	2A_SRX3-	Negative transmission data of Second pixel 3.	
36	2A_SRX3+	Positive transmission data of Second pixel 3.	
37	2A_SRX4-	Negative transmission data of Second pixel 4.	
38	2A_SRX4+	Positive transmission data of Second pixel 4.	
39	2A_FRX0-	Negative transmission data of First pixel 0.	
40	2A_FRX0+	Positive transmission data of First pixel 0.	
41	2A_FRX1-	Negative transmission data of First pixel 1.	
42	2A_FRX1+	Positive transmission data of First pixel 1.	
43	2A_FRX2-	Negative transmission data of First pixel 2.	
44	2A_FRX2+	Positive transmission data of First pixel 2.	
45	2A_FCLK-	Negative of First clock.	
46	2A_FCLK+	Positive of First clock.	
47	2A_FRX3-	Negative transmission data of First pixel 3.	



48	2A_FRX3+	Positive transmission data of First pixel 3.	
49	2A_FRX4-	Negative transmission data of First pixel 4.	
50	2A_FRX4+	Positive transmission data of First pixel 4.	
51	GND	Ground.	

CN7 Connector Pin Assignment

Pin No.	Name	Description	Note
1	GND	Ground.	
2	1B_SRX0-	Negative transmission data of Second pixel 0.	
3	1B_SRX0+	Positive transmission data of Second pixel 0.	
4	1B_SRX1-	Negative transmission data of Second pixel 1.	
5	1B_SRX1+	Positive transmission data of Second pixel 1.	
6	1B_SRX2-	Negative transmission data of Second pixel 2.	
7	1B_SRX2+	Positive transmission data of Second pixel 2.	
8	1B_SCLK-	Negative of Second clock.	
9	1B_SCLK+	Positive of Second clock.	
10	1B_SRX3-	Negative transmission data of Second pixel 3.	
11	1B_SRX3+	Positive transmission data of Second pixel 3.	
12	1B_SRX4-	Negative transmission data of Second pixel 4.	
13	1B_SRX4+	Positive transmission data of Second pixel 4.	
14	1B_FRX0-	Negative transmission data of First pixel 0.	
15	1B_FRX0+	Positive transmission data of First pixel 0.	
16	1B_FRX1-	Negative transmission data of First pixel 1.	
17	1B_FRX1+	Positive transmission data of First pixel 1.	
18	1B_FRX2-	Negative transmission data of First pixel 2.	
19	1B_FRX2+	Positive transmission data of First pixel 2.	
20	1B_FCLK-	Negative of First clock.	
21	1B_FCLK+	Positive of First clock.	
22	1B_FRX3-	Negative transmission data of First pixel 3.	
23	1B_FRX3+	Positive transmission data of First pixel 3.	
24	1B_FRX4-	Negative transmission data of First pixel 4.	
25	1B_FRX4+	Positive transmission data of First pixel 4.	
26	GND	Ground.	
27	1A_SRX0-	Negative transmission data of Second pixel 0.	
28	1A_SRX0+	Positive transmission data of Second pixel 0.	
29	1A_SRX1-	Negative transmission data of Second pixel 1.	
30	1A_SRX1+	Positive transmission data of Second pixel 1.	
31	1A_SRX2-	Negative transmission data of Second pixel 2.	
32	1A_SRX2+	Positive transmission data of Second pixel 2.	
33	1A_SCLK-	Negative of Second clock.	
34	1A_SCLK+	Positive of Second clock.	
35	1A_SRX3-	Negative transmission data of Second pixel 3.	
36	1A_SRX3+	Positive transmission data of Second pixel 3.	
37	1A_SRX4-	Negative transmission data of Second pixel 4.	
38	1A_SRX4+	Positive transmission data of Second pixel 4.	
39	1A_FRX0-	Negative transmission data of First pixel 0.	
40	1A_FRX0+	Positive transmission data of First pixel 0.	
41	1A_FRX1-	Negative transmission data of First pixel 1.	
42	1A_FRX1+	Positive transmission data of First pixel 1.	
43	1A_FRX2-	Negative transmission data of First pixel 2.	
44	1A_FRX2+	Positive transmission data of First pixel 2.	

45	1A_FCLK-	Negative of First clock.	
46	1A_FCLK+	Positive of First clock.	
47	1A_FRX3-	Negative transmission data of First pixel 3.	
48	1A_FRX3+	Positive transmission data of First pixel 3.	
49	1A_FRX4-	Negative transmission data of First pixel 4.	
50	1A_FRX4+	Positive transmission data of First pixel 4.	
51	GND	Ground.	

Note (1) CN6&CN7 connector part no.: B-F,FI-RE51S-HF, JAE Taiwan.

6.2. TFT LCD MODULE POWER INPUT

CN3 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	VIN	+18.0V power supply	
2	VIN	+18.0V power supply	
3	V5VC	+5.0V power supply	
4	V5VC	+5.0V power supply	
5	V5VC	+5.0V power supply	
6	MODE0	Format selection	(3)
7	V5VC	+5.0V power supply	
8	MODE1	Format selection	(3)
9	V5VC	+5.0V power supply	
10	NC	Not connection	
11	GND	Ground	
12	NC	Not connection	
13	GND	Ground	
14	NC	Not connection	
15	LVDS8b	8bit/10bit LVDS input selection	(4)
16	ODSEL	Overdrive Lookup Table Selection	(2)
17	GND	Ground	
18	GND	Ground	
19	GND	Ground	
20	GND	Ground	

Note (1) CN3 connector part no.: S20B-PHDSS-B(LF)(SN), JST(日本壓著端子), 德通端子 or equivalent.

Note (2) ODSEL (Overdrive Lookup Table Selection). The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

[Dino Hint: It is suggested ODSEL pin cancel in our product spec.]

ODSEL	Description
L(default)	Lookup table was optimized for 60 Hz frame rate input.
H	Lookup table was optimized for 50 Hz frame rate input.

L: Connect to GND, H: Connect to +3.3V

Note (3) Display format selection Table

Display format	MODE0	MODE1	Resolution	Note
Mode0	0	0	1920x1080x4	(b)
Mode1	1	0	1920x2160x2	(a)
Mode2	0	1	960x2160x4	
Mode3	1	1	960x2160x4	

(a) 0 : Connect to GND, 1 : Connect to +3.3V (Min:3V Max 3.6V; overshoot voltage should be less than 4V, duration: 20ns)

(b) The default format is Mode0 when the MODE0&MODE1 are no connection.



(c) Mode3 is selected as Mode2 without buffer.

Note (4) 8bit/10bit LVDS input selection

LVDS8b	Bit depth
H	8bit
L(default)	10bit

L : Connect to GND, H : Connect to +3.3V

Note (5) "L" and "H" operation in (3) could follow "CMOS Interface" in Section 4.1

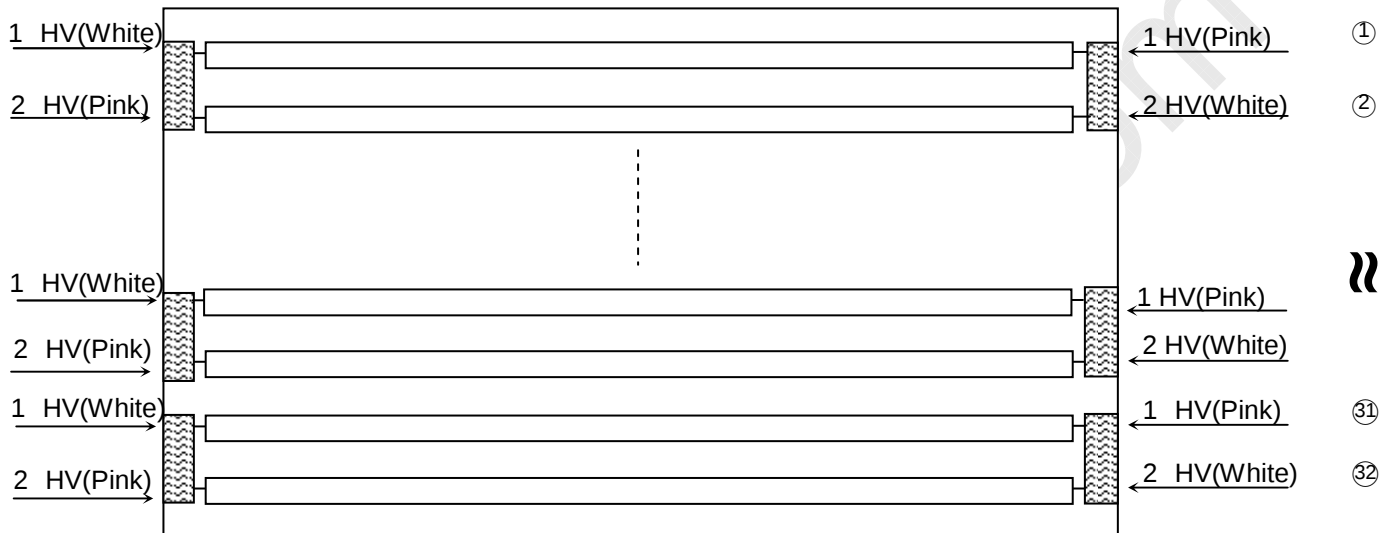
6.3. BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN8-CN23: BHR-04VS-1 (JST).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST and the mating header on inverter part number is SM02 (12.0) B-BHS-1-TB (LF).



6.4. INVERTER UNIT

CN1 (Master, Header): S14B-PH-SM4-TB (D)(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	VBL	+24V _{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	SEL	Internal/External PWM selection High : external dimming Low : internal dimming
12	E_PWM	External PWM control signal
13	I_PWM	Internal PWM Control Signal
14	BLON	Backlight on/off control

CN2 (Slave, Header): S12B-PH-SM4-TB (D)(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	VBL	+24V _{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN8-CN15 (Master, Header), CN16-CN23 (Slave, Header): SM02 (12.0) B-BHS-1-TB (LF)(JST) or equivalent

Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage



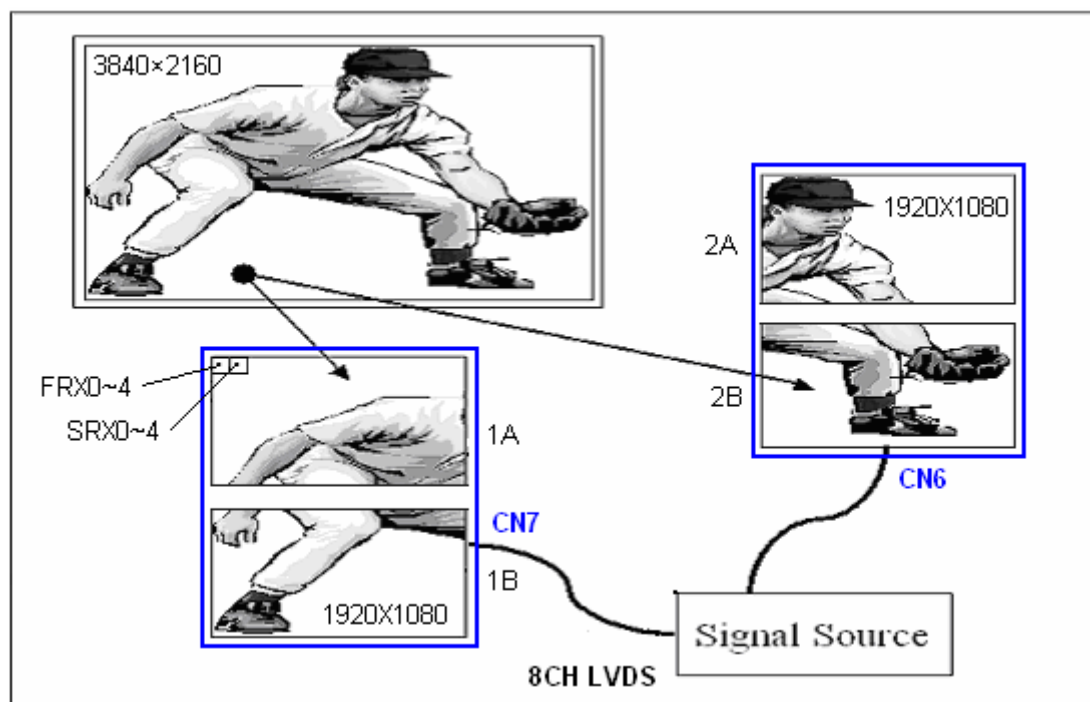
CN3-CN4 (Master, Header), CN5-CN7 (Slave, Header): 528521070 (Molex)

Pin No.	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board
9		Board to Board
10		Board to Board

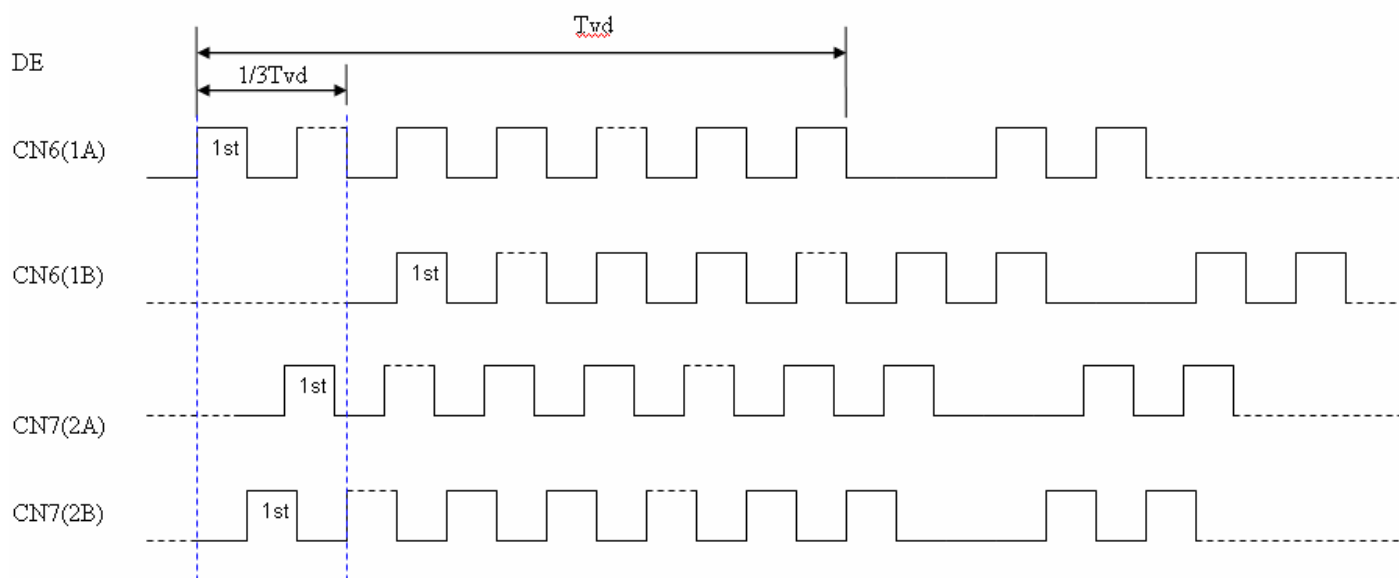
Note (1) Floating of any control signal is not allowed.

6.5. BLOCK DIAGRAM OF IMAGE SIGNAL

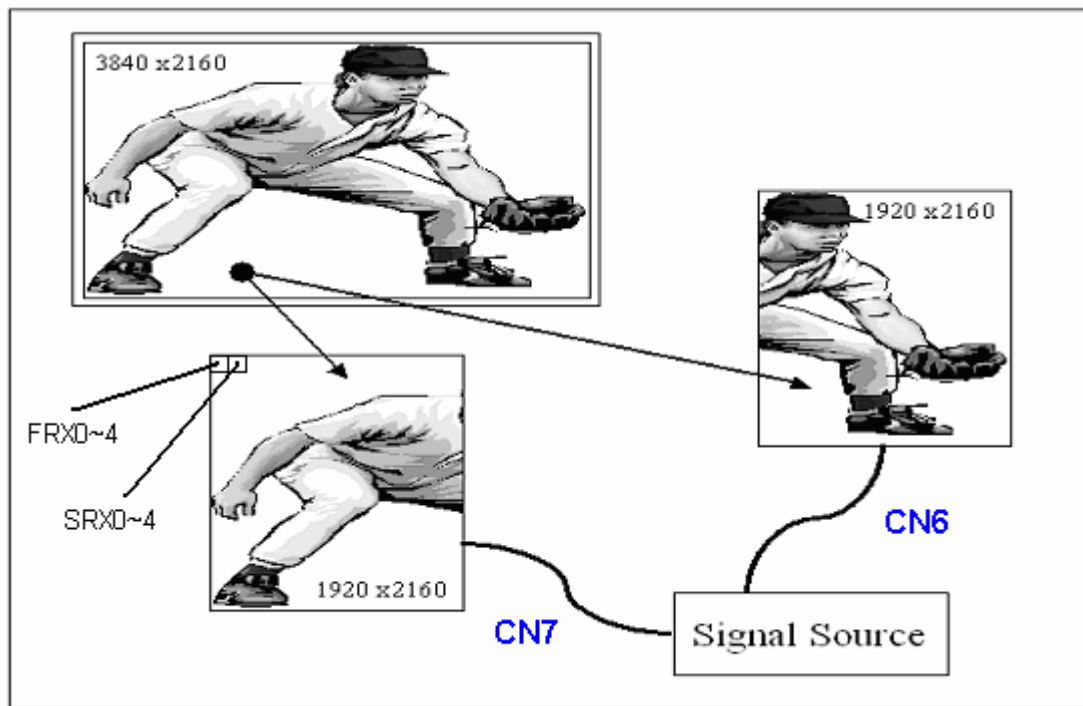
Mode 0: The video picture (3840x2160) should be divided into four parts: the left up side (1920x1080), the left down side (1920x1080), the right up side (1920x1080) and the right down side (1920x1080). Signals of these four parts should be delivered into the module individually through each 2-channel LVDS interface. But it must be "synchronous" mutually between signals from these four 2-channel LVDS interfaces. And the protocol is specified in the LVDS interface specification.



Note (1) It exists 1/3 frame buffer (i.e. buffer = $\frac{1}{3} \times 1920 \times 1080$ pixels) among CN6(2A), CN6(2B), CN7(1A) and CN7(1B) each other

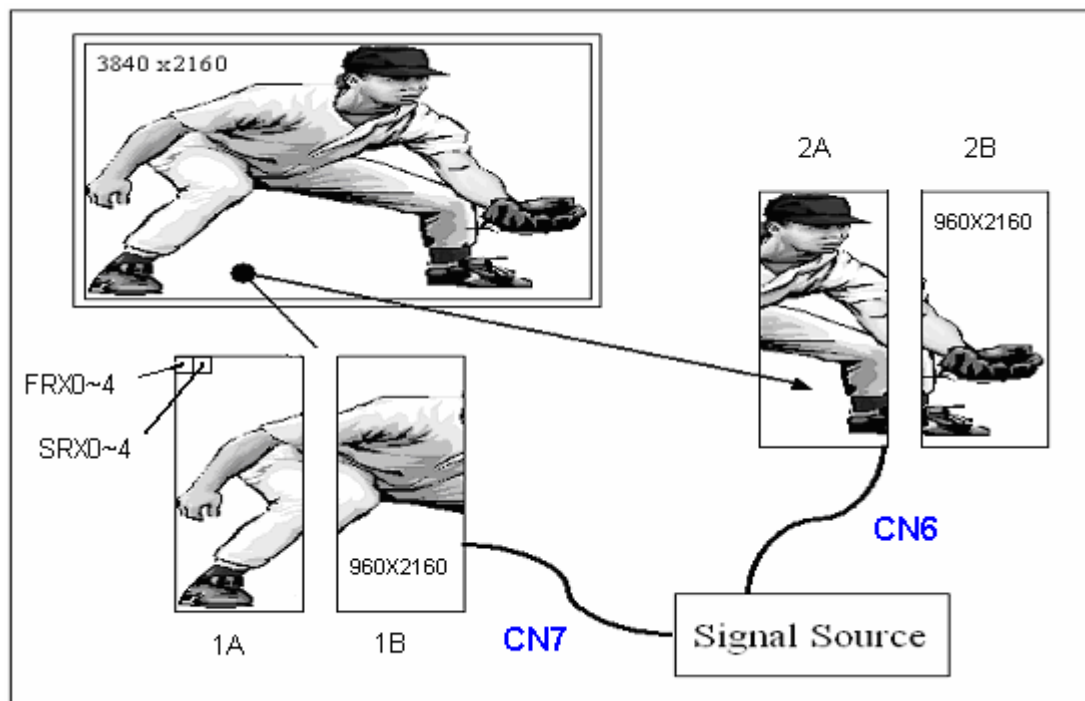


Mode1: The video picture (3840x2160) should be divided into two parts: The left side (1920x2160) and the right side (1920x2160). Signals of these two parts should be delivered into the module individually through each 2-channel LVDS interface. But it must be “synchronous” mutually between signals from these four 2-channel LVDS interfaces. And the protocol is specified in the LVDS interface specification.



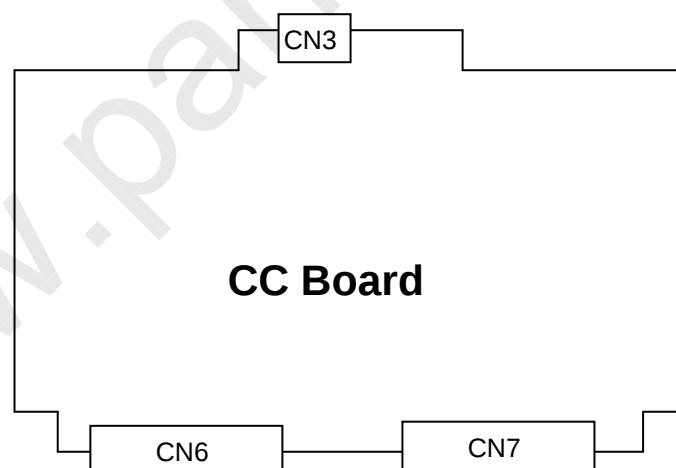
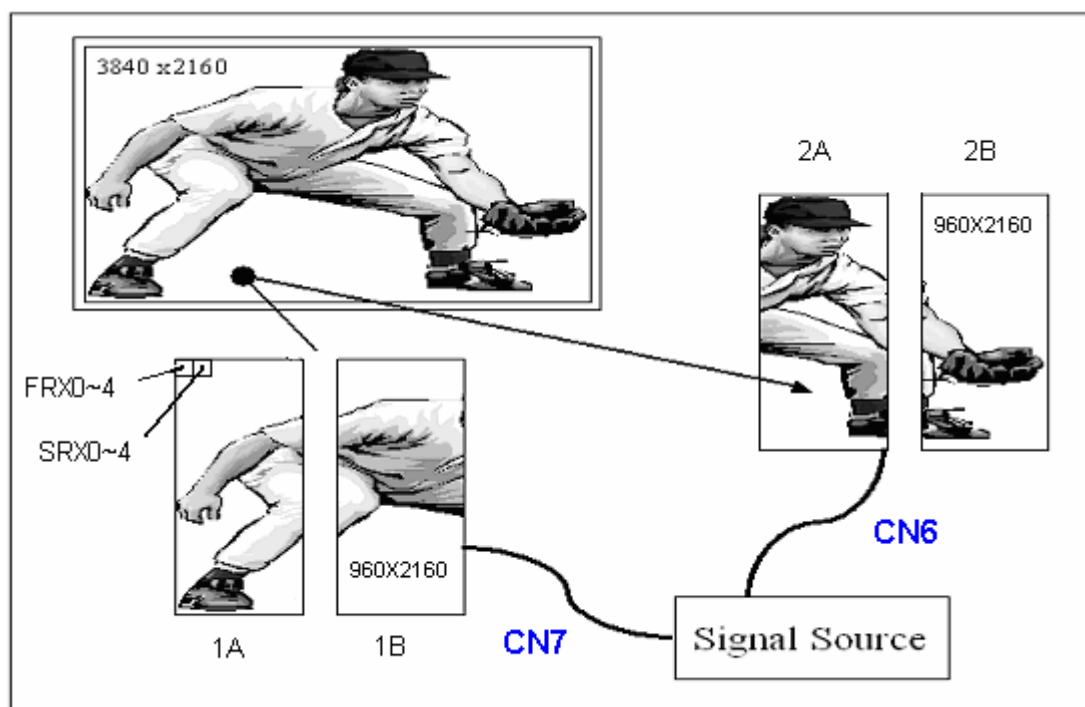
Note (1) It exists 1/3 frame buffer (i.e. buffer = $\frac{1}{3} \times 1920 \times 2160$ pixels) between CN6 and CN7

Mode2: The video picture (3840x2160) should be divided into four parts: each one is 960x2160 resolution. Signals of these four parts should be delivered into the module individually through each 2-channel LVDS interface. But it must be “synchronous” mutually between signals from these four 2-channel LVDS interfaces. And the protocol is specified in the LVDS interface specification.



Note (1) It exists 1/3 frame buffer (i.e. buffer = $\frac{1}{3} \times 960 \times 2160$ pixels) among CN6(2A),CN6(2B),CN7(1A) and CN7(1B) each other.

Mode 3: The video picture (3840x2160) should be divided into four parts: each one is 960x2160 resolution. Signals of these four parts should be delivered into the module individually through each 2-channel LVDS interface. But it must be “synchronous” mutually between signals from these four 2-channel LVDS interfaces. And the protocol is specified in the LVDS interface specification.

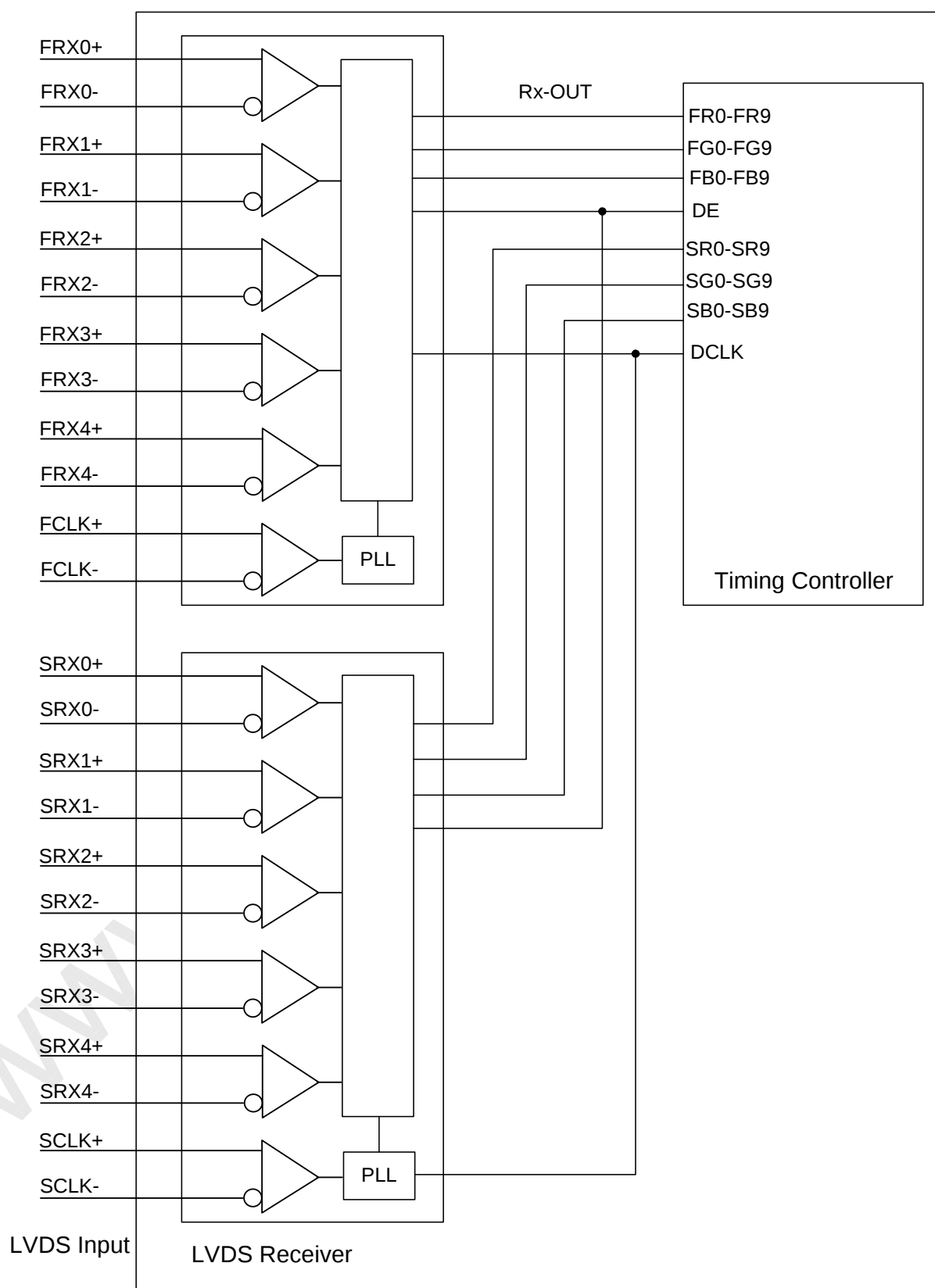


Note (1) It must be “synchronous” mutually between signals from CN6(2A) and CN6(2B).

Note (2) It must be “synchronous” mutually between signals from CN7(1A) and CN7(1B).

Note (3) It must be “synchronous” mutually between CN6 and CN7 for no frame buffer mode.

6.6. BLOCK DIAGRAM OF L.V.D.S.





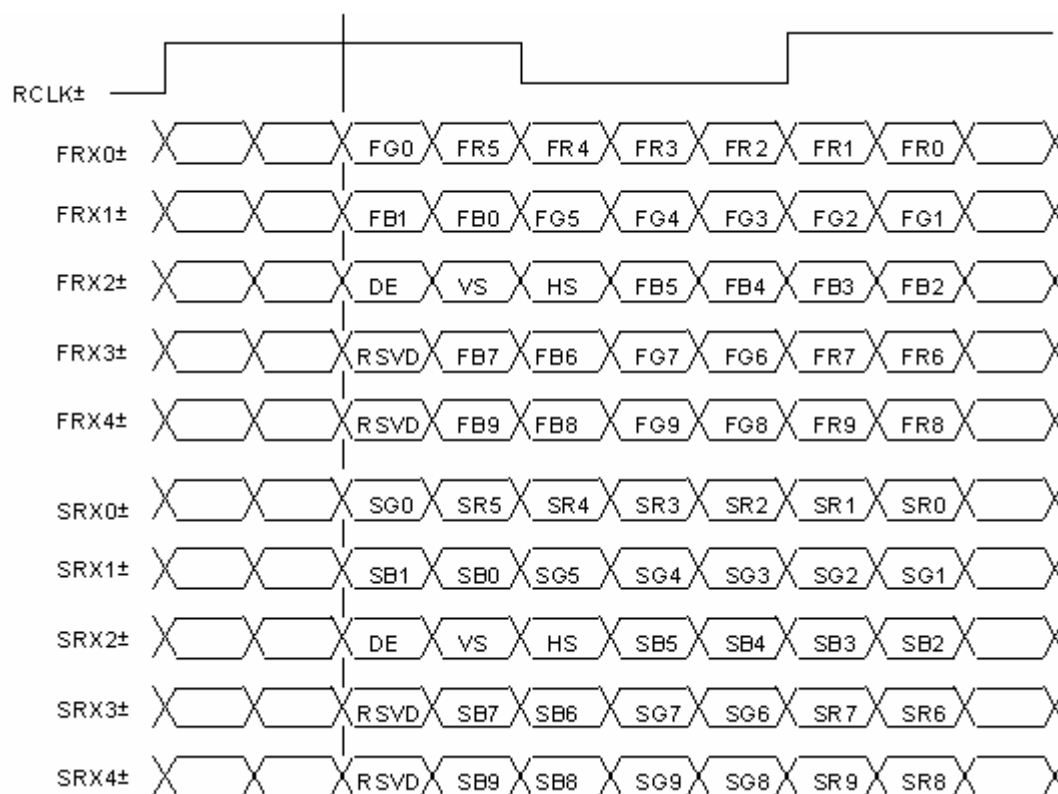
FR0~FR9	First pixel R data	SR0~SR9	Second pixel R data
FG0~FG9	First pixel G data	SG0~SG9	Second pixel G data
FB0~FB9	First pixel B data	SB0~SB9	Second pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

Note (1) The driving system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

Note (3) Two pixel data are sent into the module for every clock cycle.

6.7. L.V.D.S. INTERFACE



R0~R9 : Pixel R Data (9; MSB, 0; LSB)

G0~G9 : Pixel G Data (9; MSB, 0; LSB)

B0~B9 : Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

RCLK : Data clock signal

Note (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

6.8. COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color.

The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																														
		Red										Green										Blue										
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

7. TIMING REQUIREMENTS OF IMAGE SIGNAL

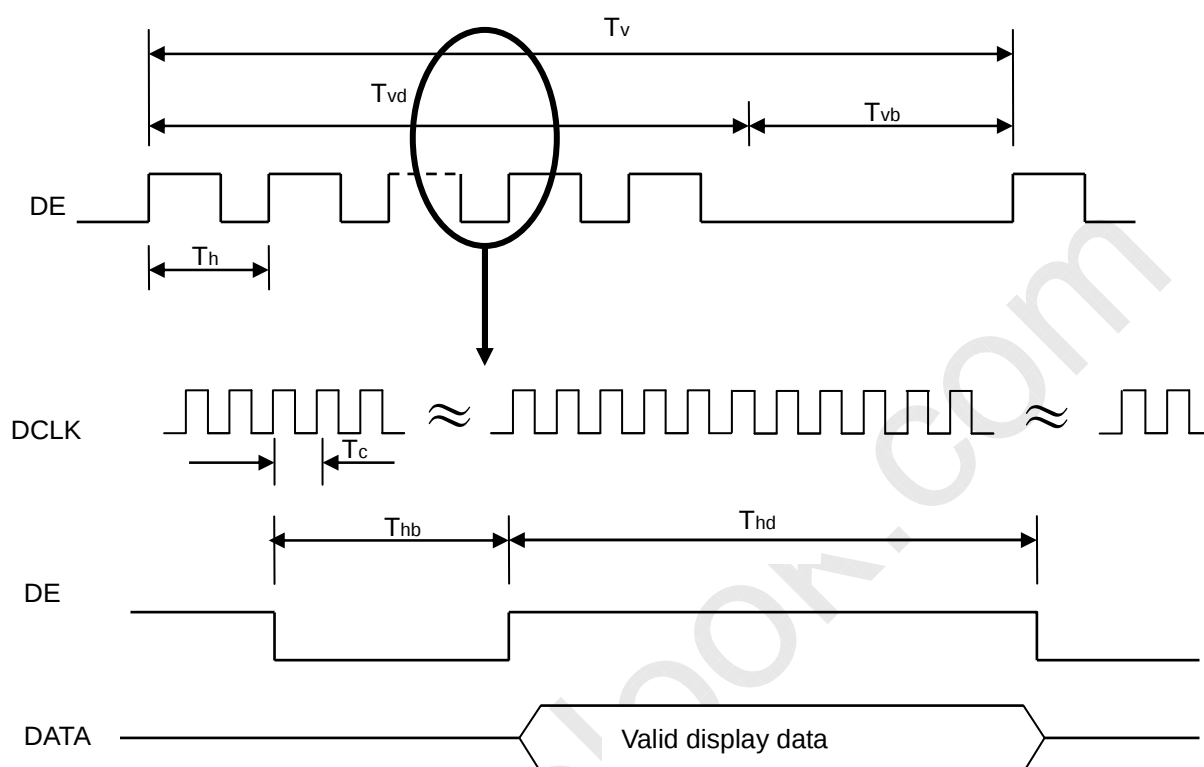
7.1. INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

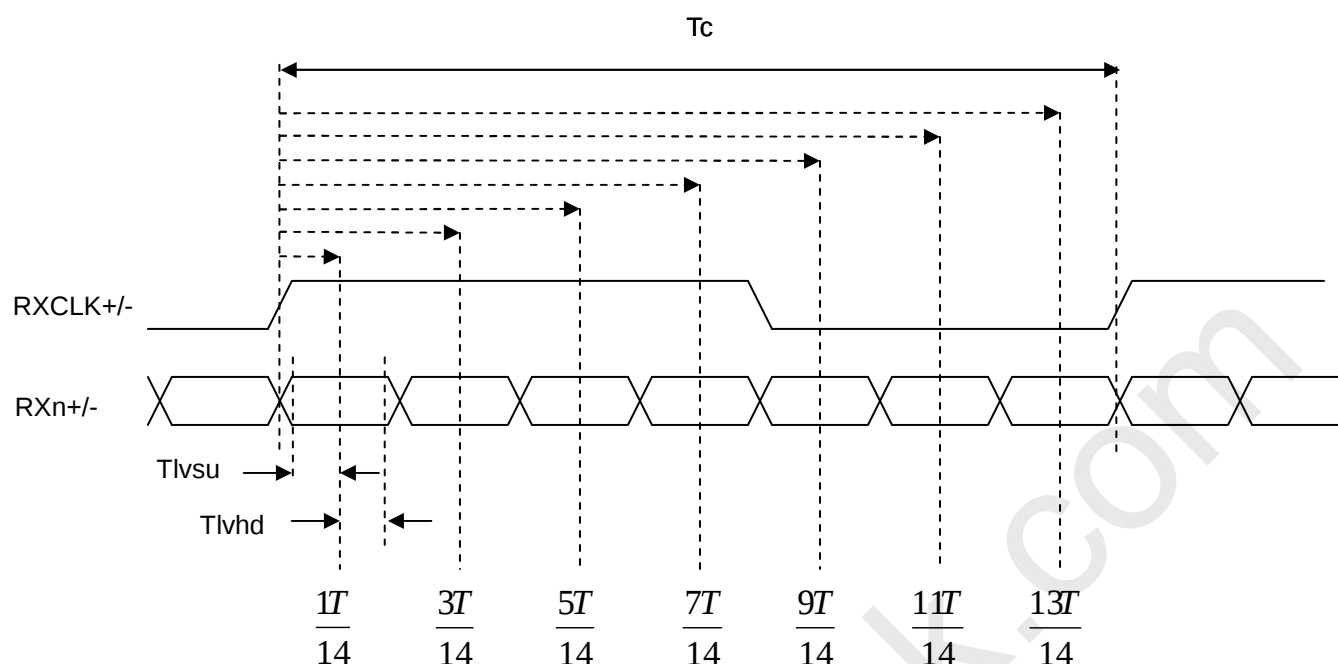
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Input cycle to cycle jitter	T_{rci}	—	—	200	ps	(3)
LVDS Receiver Data	Setup Time	T_{lvsu}	600	—	—	ps	
	Hold Time	T_{lvhd}	600	—	—	ps	
Frame rate	Frame Rate	F_{r5}	47	50	53	Hz	
		F_{r6}	57	60	62	Hz	
Mode0 LVDS Receiver Clock	Frequency	F_{r5}	65	74.25	75	MHz	(1) (2)
Vertical Active Display Term (2-CH LVDS, 1920X1080 Active Area)	Total	T_v	1110	1125	1135 (1380)	Th	$T_v = T_{vd} + T_{vb}$
	Display	T_{vd}	1080	1080	1080	Th	
	Blank	T_{vb}	30	45	55 (300)	Th	
Horizontal Active Display Term (2-CH LVDS, 1920X1080 Active Area)	Total	T_h	2190	2200	2300	Tc	$T_h = T_{hd} + T_{hb}$
	Display	T_{hd}	1920	1920	1920	Tc	
	Blank	T_{hb}	270	280	380	Tc	
Mode1 LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	70	74.25	74.5	MHz	(1) (2)
Vertical Active Display Term (2-CH LVDS, 1920x 2160 Active Area)	Total	T_v	2200	2250	2300	Th	$T_v = T_{vd} + T_{vb}$
	Display	T_{vd}	2160	2160	2160	Th	
	Blank	T_{vb}	40	90	140	Th	
Horizontal Active Display Term (2-CH LVDS, 1920x 2160 Active Area)	Total	T_h	2160	2200	2280	Tc	$T_h = T_{hd} + T_{hb}$
	Display	T_{hd}	1920	1920	1920	Tc	
	Blank	T_{hb}	240	280	360	Tc	
Mode2 LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	70	74.25	75	MHz	(1) (2)
Vertical Active Display Term (2-CH LVDS, 960x 2160 Active Area)	Total	T_v	2220	2250	2400	Th	$T_v = T_{vd} + T_{vb}$
	Display	T_{vd}	2160	2160	2160	Th	
	Blank	T_{vb}	60	90	240	Th	
Horizontal Active Display Term (2-CH LVDS, 960x 2160 Active Area)	Total	T_h	1090	1100	1760	Tc	$T_h = T_{hd} + T_{hb}$
	Display	T_{hd}	960	960	960	Tc	
	Blank	T_{hb}	130	140	340	Tc	
Mode3 LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	78	80	80	MHz	(1) (2)
Vertical Active Display Term (2-CH LVDS, 960x 2160 Active Area)	Total	T_v	2164	2222	2600	Th	$T_v = T_{vd} + T_{vb}$
	Display	T_{vd}	2160	2160	2160	Th	
	Blank	T_{vb}	4	62	440	Th	
Horizontal Active Display Term (2-CH LVDS, 960x 2160 Active Area)	Total	T_h	1194	1200	1400	Tc	$T_h = T_{hd} + T_{hb}$
	Display	T_{hd}	960	960	960	Tc	
	Blank	T_{hb}	234	240	460	Tc	

Note (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM



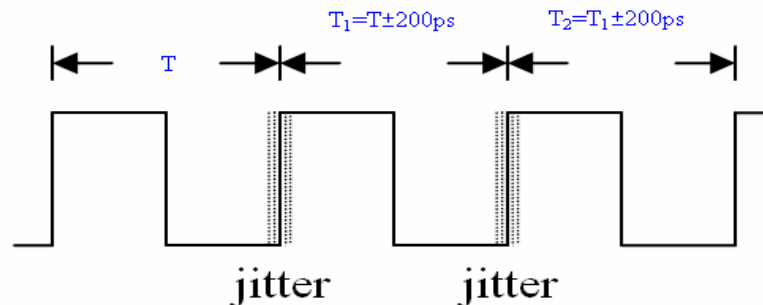
LVDS RECEIVER TIMING DIAGRAM



Note (2) Please make sure the range of frame rate has follow the below equation :

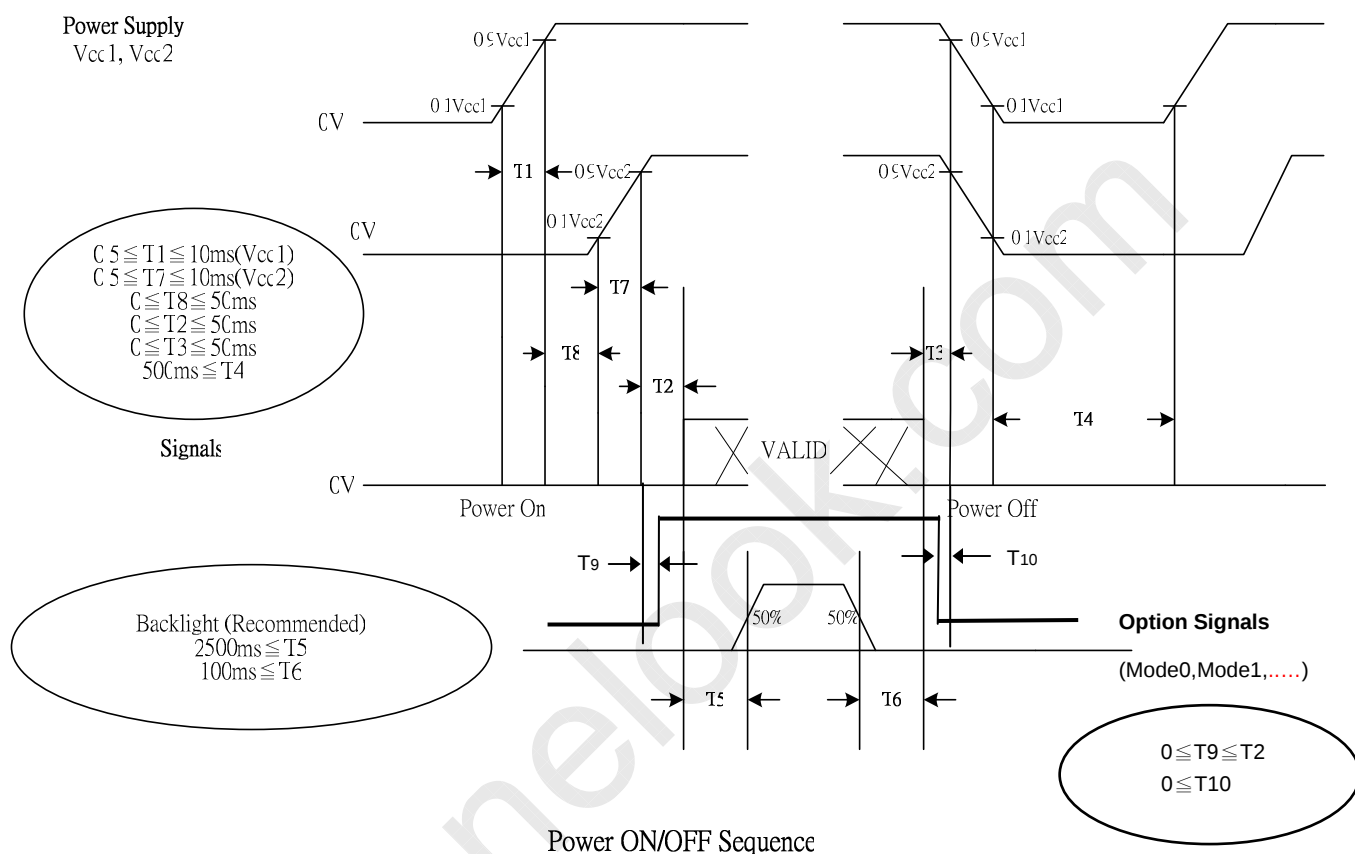
$$Fr(max) \geq Fclkin \quad / \quad T_v \times T_h \leq Fr(min)$$

Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T|$



7.2. POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be followed as the diagram below.



Note (1) The supplied voltage of the external system for the module input should follow the definition of Vcc1,2.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc1,2 is in off level, please keep the level of input signals on the low and avoid floating.

Note (4) T4 should be measured after the module being fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

8. OPTICAL CHARACTERISTICS

8.1. TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Frame Rate	F _r	60	Hz

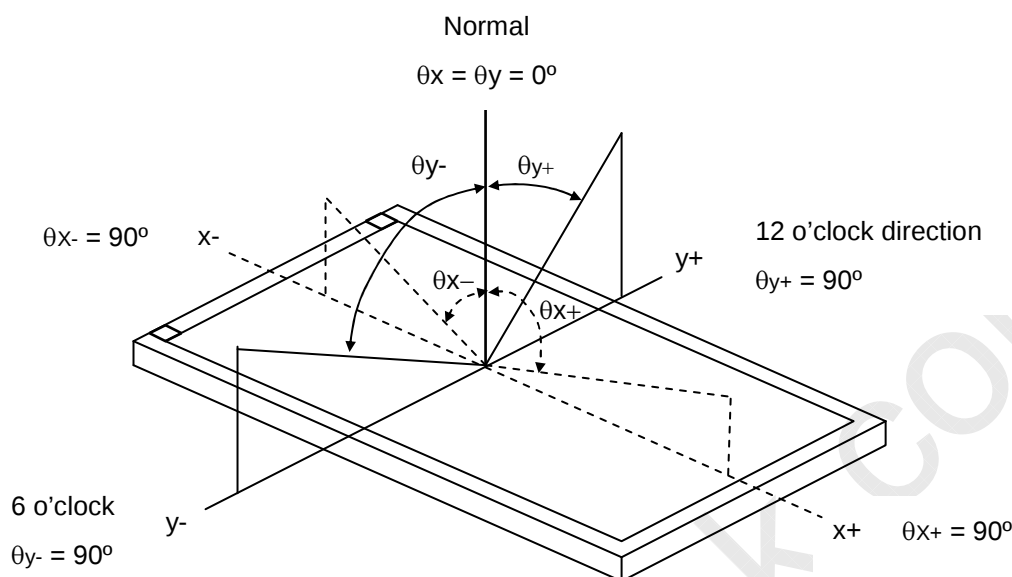
8.2. OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 8.2 Notes. The following items should be measured under the test conditions described in 8.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at normal direction	900	1200		-	Note (2)
Response Time		Gray to gray			6.5	12	ms	Note (3)
Center Luminance of White		L _c		400	450		cd/m ²	Note (4)
White Variation		δW				1.6	-	Note (7)
Cross Talk		CT				2	%	Note (5)
Color Chromaticity	Red	R _x		Typ. -0.03	0.663	Typ. +0.03	-	Note (6)
		R _y			0.330		-	
	Green	G _x			0.184		-	
		G _y			0.691		-	
	Blue	B _x			0.149		-	
		B _y			0.043		-	
	White	W _x			0.280		-	
		W _y			0.290		-	
	Color Gamut	C.G		95	100		%	NTSC
Viewing Angle	Horizontal	θ_{x+}	CR≥30	80	88		Deg.	Note (1)
		θ_{x-}		80	88			
	Vertical	θ_{y+}		80	88			
		θ_{y-}		80	88			

Note (1) Definition of Viewing Angle (θ_x , θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

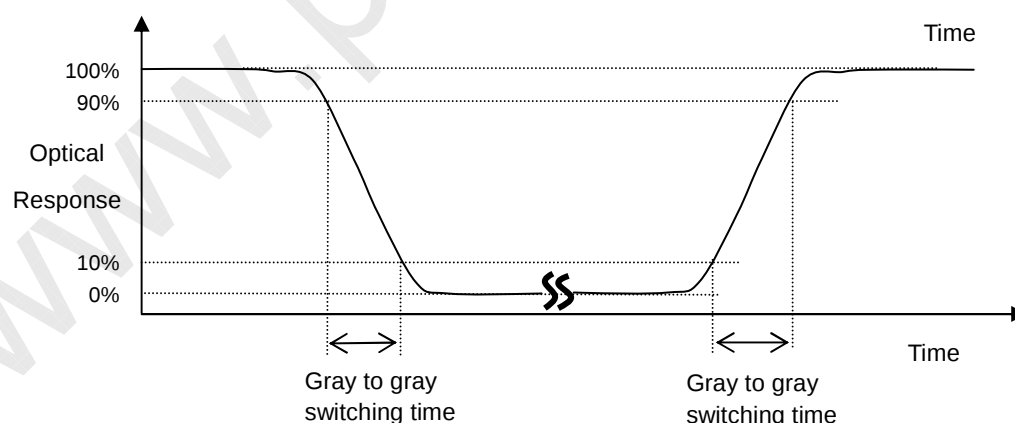
$$\text{Contrast Ratio (CR)} = L_{1023} / L_0$$

L_{1023} : Luminance of gray level 1023

L_0 : Luminance of gray level 0

$CR = CR(7)$, where $CR(X)$ is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892, and 1023. Gray to gray. Average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892, and 1023 to each other.

Note (4) Definition of Luminance of White (L_c):

Measure the luminance of gray level 1023 at center point

$$L_c = L(7)$$

Where $L(x)$ is corresponding to the luminance of the point X at the figure in Note (7).

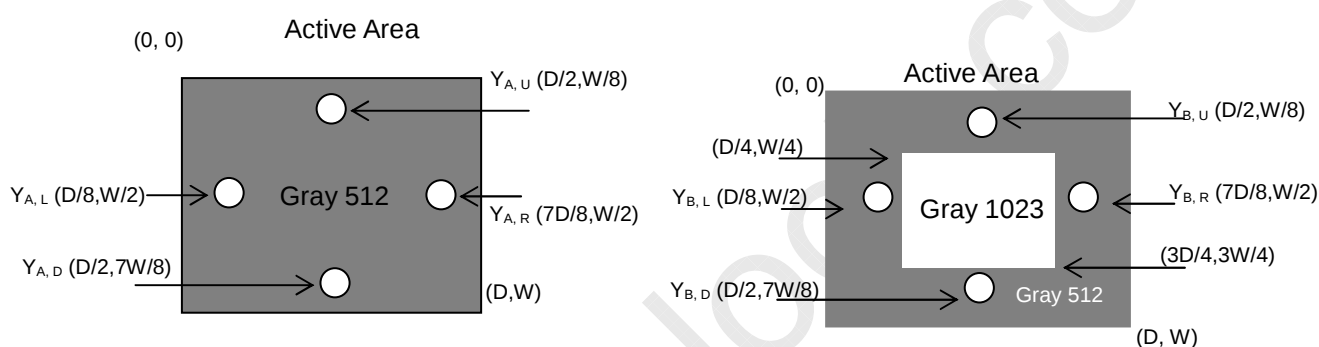
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

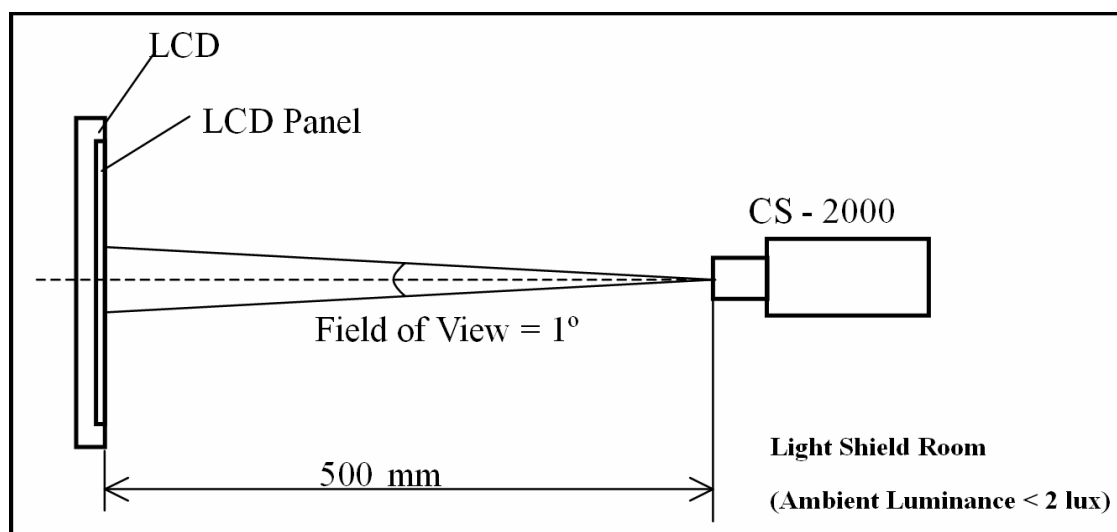
Y_A = Luminance of measured location without gray level 1023 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 1023 pattern (cd/m^2)



Note (6) Measurement Setup:

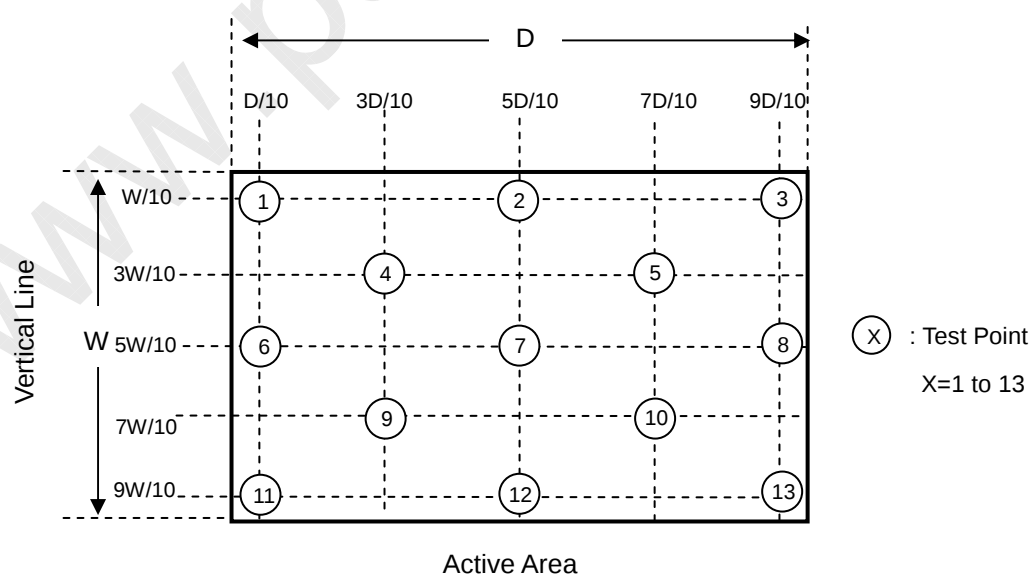
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 512 at 13 points

$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), \dots, L(13)] / \text{Minimum} [L(1), L(2), L(3), L(4), \dots, L(13)]$$



9. PRECAUTIONS

9.1. ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.
- (6) Do not plug in or pull out the I/F connector while the module is in operation.
- (7) Do not disassemble the module.
- (8) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (9) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (10) When storing modules as spares for a long time, the following precaution is necessary.
 - a. Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
 - b. The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- (11) When ambient temperature is lower than 10 °C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

9.2. SAFETY PRECAUTIONS

- (1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

9.3. SAFETY STANDARDS

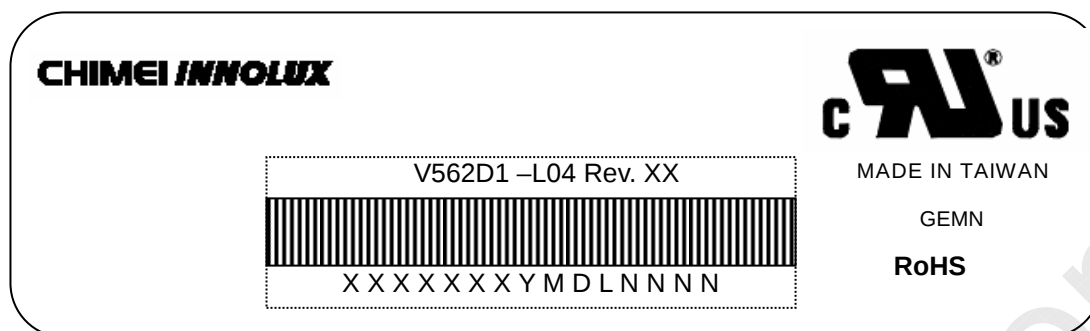
The LCD module should be certified with safety regulations as follows:

- (1) UL60950-1 or updated standard.
- (2) IEC60950-1 or updated standard.
- (3) UL60065 or updated standard.
- (4) IEC60065 or updated standard.

10. DEFINITION OF LABELS

10.1. CMI MODULE LABEL

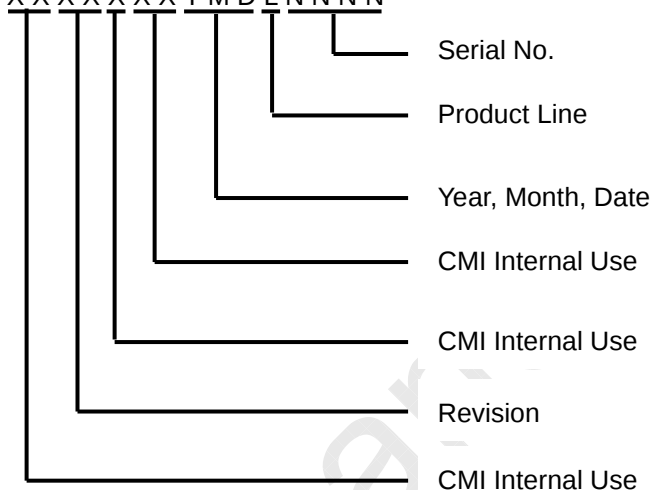
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V562D1-L04

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4...2010=0, 2011=1, 2012=2...

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

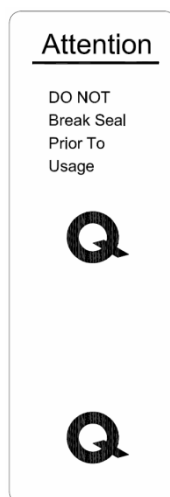
Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, ...etc.

10.2. WARRANTY LABEL

Warranty labels are pasted on the rear of the BLU. This warranty label is defined to be recognized if the module ever disassembled or not. If the module was dismounted, then it will be out of warranty. When remove the warranty label, there are prints will remain on the surface of the BLU. If the label was removed or it has the imprint by tearing, it will be treated as disassembled.



11. PACKAGING

11.1. PACKING SPECIFICATIONS

- (1) 2 LCD TV modules / 1 Box
- (2) Box dimensions : 1448(L) X 372 (W) X 901 (H)
- (3) Weight : approximately 56Kg (2 modules per box)
- (4) One protective film is attached on the LCD TV

11.2. PACKING METHOD

Figures 11-1 and 11-2 are the packing method

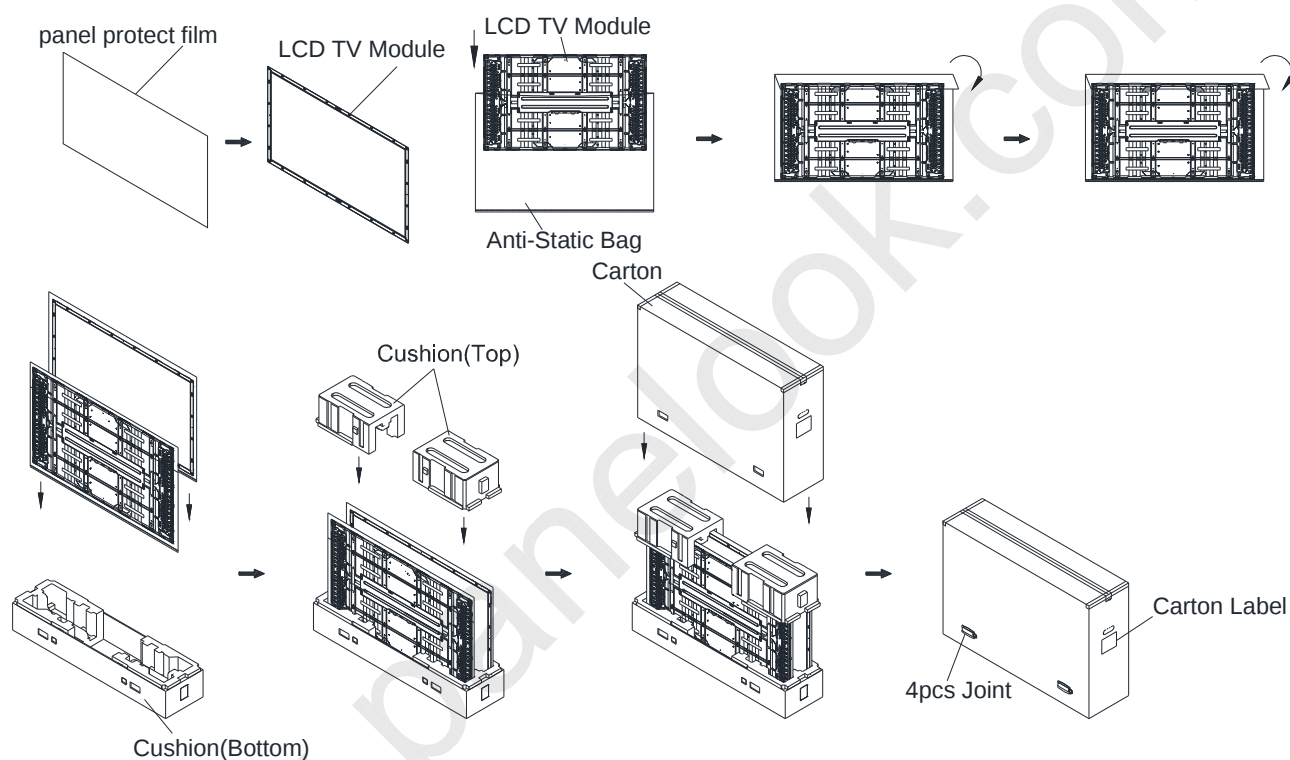


Figure.11-1 packing method

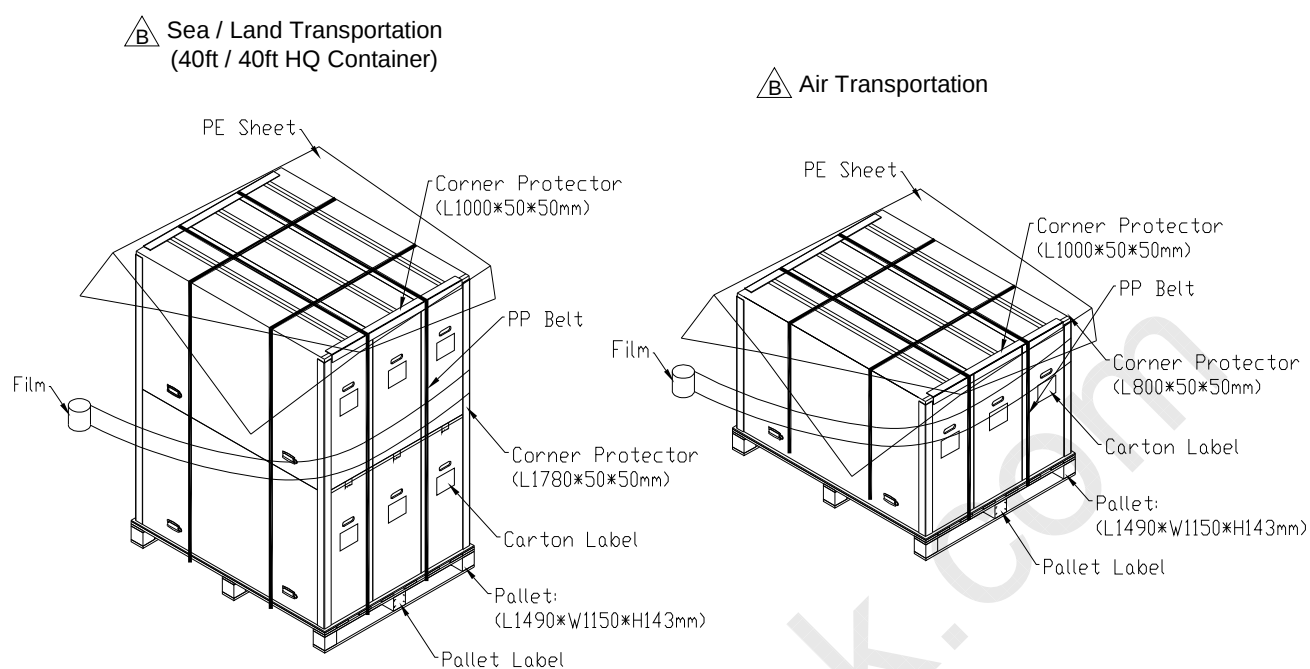
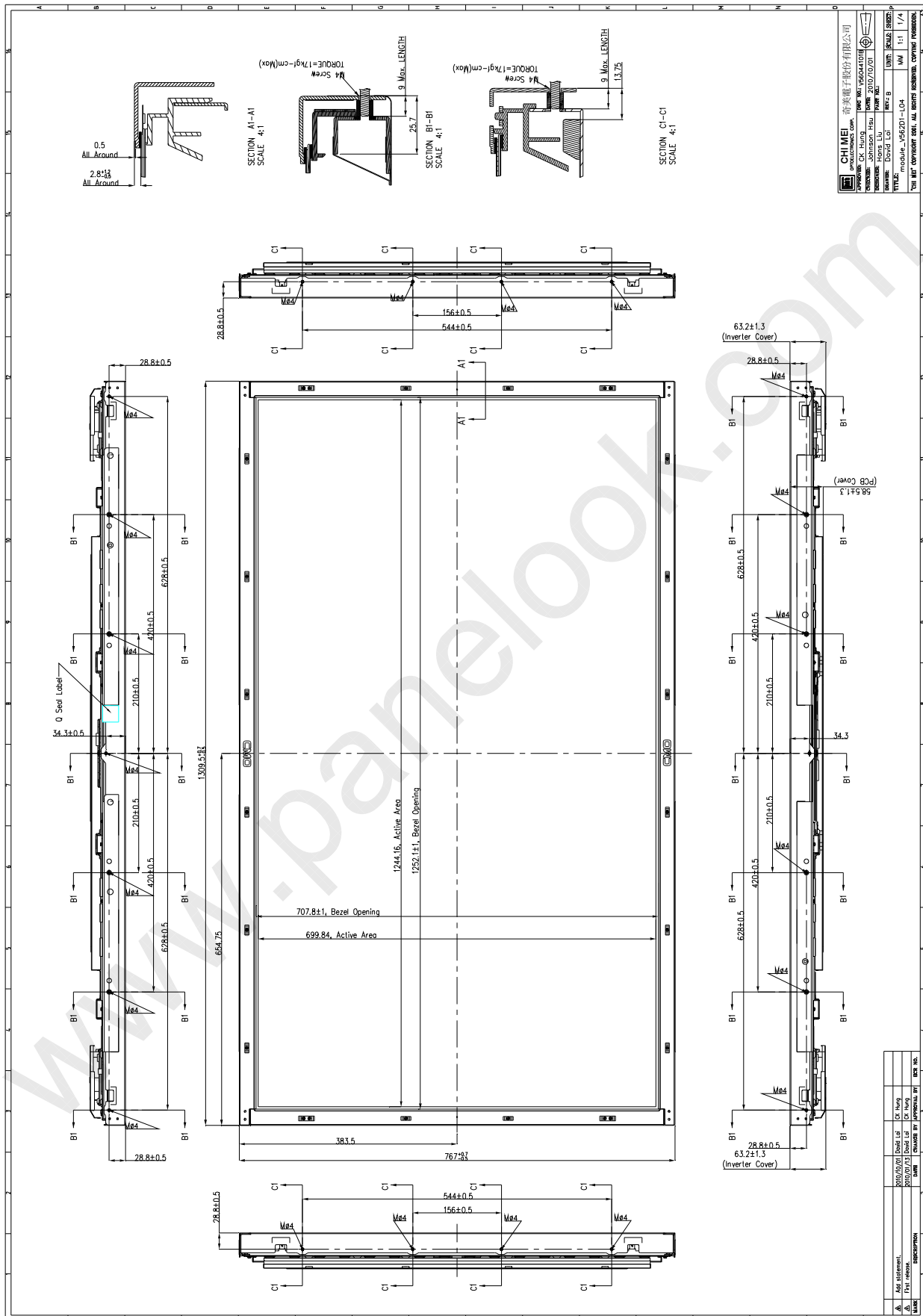
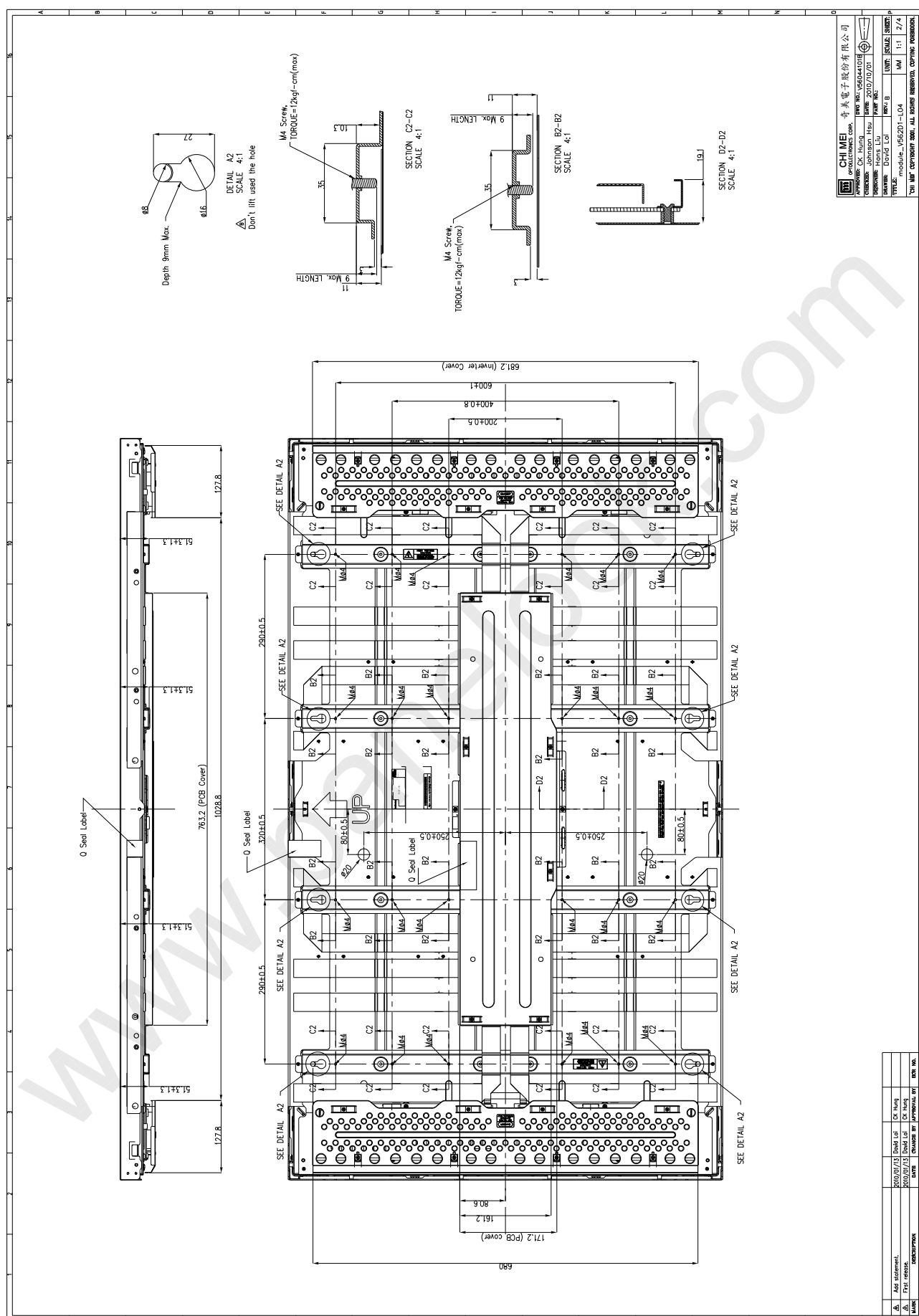


Figure.11-2 Packing method

12. MECHANICAL CHARACTERISTIC



PRODUCT SPECIFICATION



PRODUCT SPECIFICATION

